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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,822	05/14/2001	Michael James	6950-60281 (0008856.0002)	9659

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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	8

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,822	JAMES ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Original claims 1-24 are pending.

Claim Objections

2. Claim 6 is objected to because of the following informalities: "provide" is interpreted as –provided--. Appropriate correction is required.

3. Claim 7 is objected to because of the following informalities: "over the message but" is interpreted as –over the message bus--; on line 3, "and" is interpreted as –or--. Appropriate correction is required.

4. Claim 8 is objected to because of the following informalities: one line 3, "and" is interpreted as –or--. Appropriate correction is required.

5. Claim 14 is objected to because of the following informalities: "over the message" is interpreted as –over the message bus--; on line 4, "and" is interpreted as –or--. Appropriate correction is required.

6. Claim 15 is objected to because of the following informalities: one line 4, "and" is interpreted as –or--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-15 and 20-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Bell et al., U.S. Patent No. 6,658,579 ("Bell").

As per claim 1, Bell discloses a timing circuit for use with transport logic in a network element (Fig. 40 & Fig. 41a, external controller cards 542b & 543b for use in network device 540; Fig. 49, external controllers include external central timing subsystems (EX CTS) 750), the network element forms part of a data network, the timing circuit comprising:

a timing receiver having a timing input, timing output, and a selection input, the timing receiver operable to receive one or more timing signals at the timing input and to select a selected timing signal for distribution to the transport logic via the timing output based on a selection signal received at the selection input (Figs. 50a-c, timing inputs 770 and STRAT_SYNC, selection input REF_SEL[1:0], and timing output 781; Col. 75, lines 24-32, distribution to transport logic);

a determination circuit operable to determine whether the timing circuit is one of a master timing circuit and slave timing circuit, and based on the determination, produce the selection signal (Fig. 50b, hardware control logic 760; Col. 77, lines 18-27); and

a sync transmitter coupled to the timing output, the determination circuit, and a communications channel, the sync transmitter operable to receive the selected timing signal and to transmit the selected timing signal on the communication channel when the determination circuit determines that the timing circuit is the master timing circuit (Fig. 50c, External Reference Clock (ERC) circuit 782; Col. 78, lines 10-33).

As per claim 2, Bell discloses the one or more timing signals include a client synchronization signal associated with client data that is to be transported on the data network (Col. 75, lines 3-11, port timing signals 753).

As per claim 3, Bell discloses when the determination circuit determines that the timing circuit is the master timing circuit, the selection signal is generated to select the client synchronization signal associated with client data for distribution to the transport logic (Col. 75, lines 12-23).

As per claim 4, Bell discloses the timing receiver is coupled to the communication channel and the one or more timing signals include a master sync signal received on the communication channel (Col. 75, lines 3-11, external timing reference signal 755)..

As per claim 5, Bell discloses when the determination circuit determines that the timing circuit is the slave timing circuit, the selection signal is generated to select the master sync signal associated with client data for distribution to the transport logic (Col. 75, lines 12-23).

As per claim 6, Bell discloses the one or more timing signals include an external sync provided at the network element (Col. 75, lines 3-11, BITS lines 751).

As per claim 7, Bell discloses the determination circuit is coupled to a message bus and is operable to receive at least one message over the message bus to determine whether the timing circuit is one of the master timing circuit or the slave timing circuit (Col. 78, lines 44-49).

As per claim 8, Bell discloses the determination circuit is operable to receive at least one local parameter to determine whether the timing circuit is one of the master timing circuit or the slave timing circuit (Col. 78, lines 44-49).

As per claim 9, Bell discloses a synchronization system for use in a network element that forms part of a data network (Fig. 40, network device 540), the network element includes transport logic to transport one or more data streams in the data network (Figs. 41a-c), wherein each of the one or more data streams has an associated synchronization signal (Fig. 49), and wherein the transport logic comprises two or more circuit assemblies that are coupled together via a communication channel (Col. 58, lines 64-67, external controller cards 542b and 543b are coupled via mid-plane 622a), the synchronization system comprising:

two or more determination circuits located on the two or more circuit assemblies (Fig. 49, external controllers include external central timing subsystems (EX CTS) 750), one determination circuit per assembly (Fig. 50b, hardware control logic 760), wherein each determination circuit includes logic to determine whether its respective circuit assembly is one of a master circuit assembly and a slave circuit assembly (Col. 78, lines 44-49); and

two or more timing circuits coupled to the two or more determination circuits, one timing circuit per determination circuit, wherein each timing circuit includes logic to receive a plurality

of synchronization signals (Col. 75, lines 3-11; Figs. 50a-c) and logic to selectively transmit a selected synchronization signal of the plurality of synchronization signals over the communication channel (Col. 75, lines 24-33; Figs. 50a-c).

As per claims 10-15, since Bell discloses the timing circuit of claims 1-8 and the synchronization system of claim 9, Bell discloses the claimed synchronization system.

As per claim 20, Bell discloses a method for synchronizing transport logic in a network element that forms part of a data network (Fig. 40, network device 540; Figs. 41a-c), the transport logic is used to transport one or more data streams in the data network, wherein each of the one or data streams has an associated synchronization signal (Fig. 49), and wherein the transport logic comprises two or more circuit assemblies that are coupled together via a communication channel (Col. 58, lines 64-67, external controller cards 542b and 543b are coupled via mid-plane 622a; Fig. 49, external controllers include external central timing subsystems (EX CTS) 750), the method comprising the steps of:

determining that a selected circuit assembly is a master circuit assembly and that remaining circuit assemblies are slave assemblies (Col. 78, lines 44-49);

receiving at least one associated synchronization signal at the master circuit assembly (Col. 75, lines 3-11);

synchronizing the master circuit assembly to the at least one associated synchronization signal (Col. 75, lines 12-23);

distributing the at least one associated synchronization signal from the master circuit assembly to the slave circuit assemblies via the communication channel (Col. 58, lines 64-67; Fig. 49); and

synchronizing the slave circuit assemblies to the at least one synchronization signal (Col. 75, lines 12-23).

As per claim 21, Bell discloses a step of determining that the selected circuit assembly is a master circuit assembly and that the remaining circuit assemblies are slave circuit assemblies using a position indicator associated with the respective circuit assembly (Col. 78, lines 44-49, slot identification).

As per claims 22 and 23, since Bell discloses the timing circuit of claims 7 and 8, Bell discloses the claimed method.

As per claim 24, Bell discloses two or more circuit assemblies that are coupled together via a second communication channel (Col. 58, lines 38-41, auxiliary processor cards 542c and 543c; lines 64-67, via mid-plane 622b).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell et al., U.S. Patent No. 6,658,579 ("Bell"), in view of Cardona et al., U.S. Patent No. 6,317,439 ("Cardona").

As per claim 16, Bell teaches a synchronization system for use with a card set in a network element that forms part of an optical network (Col. 13, lines 50-55, SONET), the card set comprising first and second circuit cards operable to transport data via the optical network (Fig. 40 & Fig. 41a, external controller cards 542b & 543b for use in network device 540; Fig. 49, external controllers include external central timing subsystems (EX CTS) 750; Col. 76, lines 13-24, EX CTSs may be located on other cards), wherein that data has an associated synchronization signal, the synchronization system comprising:

a communications channel (Col. 58, lines 64-67, mid-plane);

a determination circuit operable to determine which of the first and second circuit cards is a master circuit and which is a slave circuit (Col. 78, lines 44-49, hardware controller logic 760);

a first timing circuit located on the master circuit card and coupled to the communication channel (Fig. 49, external controllers include EX CTSs 750), the first timing circuit includes logic to receive the associated synchronization signal and to synchronize the master circuit card to the associated synchronization signal (Col. 75, lines 12-23; Figs. 50a-c), the first timing circuit further including logic to transmit the associated synchronization signal over the communication channel (Col. 75, lines 24-33; Figs. 50a-c);

a second timing circuit located on the slave circuit card and coupled to the communication channel (Fig. 49, external controllers include EX CTSs 750), the second timing circuit having logic to receive the associated synchronization signal from the communication

channel and to synchronize the slave circuit card to the associated synchronization signal (Col. 75, lines 12-23; Figs. 50a-c).

However, Bell does not expressly teach that the card set is an ADM card set. Bell does teach that the timing circuit "may be located ... on any other cards in the network device" (Col. 76, lines 12-24). Cardona teaches an ADM board set comprising an active module and a standby module (Col. 4, lines 18-29). At the time of the invention, it would have been obvious to apply Bell's synchronization system to Cardona's ADM. A motivation for doing so would have been to provide fail-over capacity for the synchronization function of the ADM (Cardona, Col. 4, lines 18-29).18-29).

As per claim 17, since Bell teaches the method of claim 21, Bell/Cardona teaches the claimed synchronization system.

As per claims 18 and 19, since Bell teaches the timing circuit of claims 7 and 8, Bell/Cardona teaches the claimed synchronization system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

aw
May 13, 2004

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